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SRI VASAVI ENGINEERING COLLEGE (AUTONOMOUS)

(Sponsored by Sri Vasavi Educational Society) (Approved by AICTE, New Delhi & Recognized by UGC under section 2(f) & 12(B)) (Permanently affiliated to JNTUK, Kakinada, Accredited by NBA and NAAC with 'A' Grade) Pedatadepalli, TADEPALLIGUDEM – 534 101.W.G.Dist. (A.P)

Department of Electronics and Communication Engineering

Skill Oriented Program on

"Basic Digital Circuit Design with VHDL and

QuestaSim Tool"



Report of the Program

In our ECE Department, The SPACE Club has organized **One week Skill Oriented Program on " "Basic Digital Circuit Design with VHDL and QuestaSim Tool"** under the Scheme of SPICES, Sponsored by AICTE, New Delhi. This program was conducted during 27th MAR to 1st APR-2023.

In this program, Total 70 Members were participated as teams. The Team Size may consist of 4 to 5 students. Likewise Total 14 Teams were Formed.

Course Description:

Digital Circuit Design with VHDL and QuestaSim is a course designed to provide students with a comprehensive understanding of digital circuit design principles and techniques using VHDL and QuestaSim. The course covers the basics of digital circuits, VHDL syntax and data types, and behavioral modeling with VHDL. Students will learn how to design, simulate, and analyze combinational and sequential circuits using QuestaSim.

Day 1: Introduction to Digital Circuit

- Introduction to digital circuit design
- Overview of digital circuits and their applications
- Overview of VHDL and QuestaSim
- VHDL syntax and data types
- Behavioral modeling with VHDL
- Creation of a basic project in QuestaSim
- Day 2: Combinational Circuit Design and Simulation
- Combinational circuit design principles
- VHDL modeling of combinational circuits
- Simulation of combinational circuits using QuestaSim
- Lab: Design and simulation of a simple combinational circuit

• Day 3: Sequential Circuit Design and Simulation

- Sequential circuit design principles
- VHDL modeling of sequential circuits
- Simulation of sequential circuits using QuestaSim
- Lab: Design and simulation of a simple sequential circuit
- Day 4: State Machine Design with VHDL and Simulation
- State machine design principles
- VHDL modeling of state machines
- Simulation of state machines using QuestaSim
- Lab: Design and simulation of a simple state machine
- •

• Day 5: Advanced Topics in Digital Circuit Design and Project Work

- Using VHDL for control logic design
- Design optimization and performance analysis with QuestaSim
- Final project work, incorporating the topics covered in the previous days

Presentation of final project to the class

Day 6: Project Presentations and Wrap-Up

- Final project presentations by students
- Review of key concepts and topics covered throughout the course
- Open discussion and Q&A session
- Course evaluations and feedback

All the participants felt very happy and gave very good Feedback towards this Program.

Total amount spent by the college towards this Program :

No. of Students Registered : 70

Registration Fee Per Head : Rs 215

Total amount paid to Trainers : Rs 15,000

E. Kusmaline

Dr. E. Kusuma Kumari Professor & HOD-ECE



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Department of Electronics and Communication Engineering

Date: 11-04-2023

To The Principal, Sri Vasavi Engineering College

Sub: Request to make a SOC Program Registration fee Rs.15000/- payment - Reg

Respected Sir,

This is to bring to you kind notice that one week SOC Program on "Basic Digital Circuit Design with VHDL and QuestaSim Tool" was delivered by Mr. U. Uma Maheswara Rao, Research scholar, NIT, AP. for IV Semester ECE students organized by SPACE CLUB under the SPICES Scheme sponsored by AICTE during 27th March to 01st April 2023. In this Program total 70 members were attended. Now I am requesting you to kindly instruct the concern authority to make an arrangement of Program Registration fee payment to the trainers as given below.

Number of Students attended : 70

Each Student Registration fee: Rs. 215/-

Total amount

: Rs. 15000/-

The Bank account Details:

Ukyam Uma Maheswara Rao State Bank of India, Vetapalem 33916556395 SBIN0003264

Head of the Depart

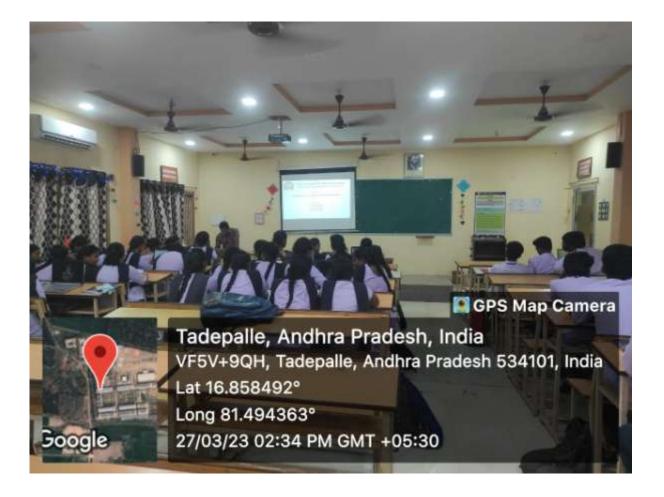
Status Enquiry

UTR Number Bank Name Branch Name IFSC Code Debit Account Number Beneficiary Account Number Transfer Amount Transfer Type Transfer Date Commission **Beneficiary Name** Beneficiary Address1 Beneficiary Address2 Beneficiary Address3 Beneficiary Address4 Status

IDIBH23103180559 STATE BANK OF INDIA VETAPALEM BRANCH SBIN0003264 CA-7048324044 33916556395 15000 NEFT 2023-04-13 16:38:58 5.61 U UMA MAHESWARA RAO

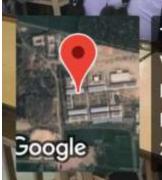
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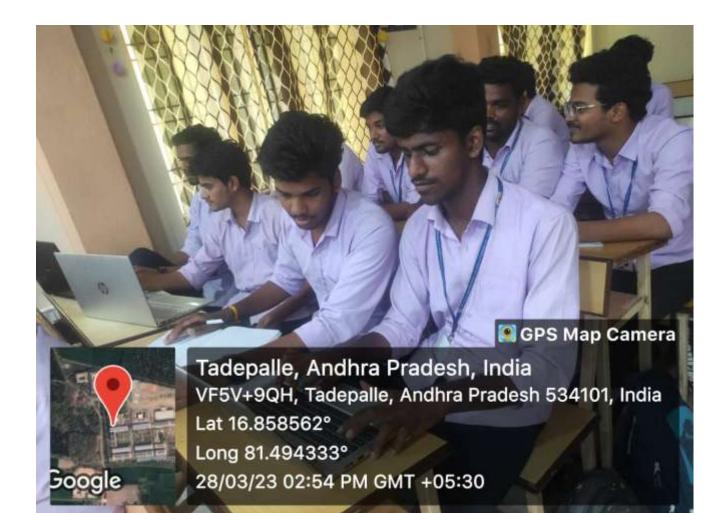








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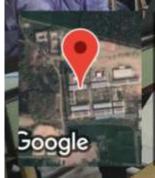


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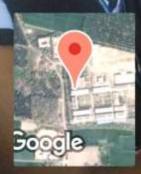


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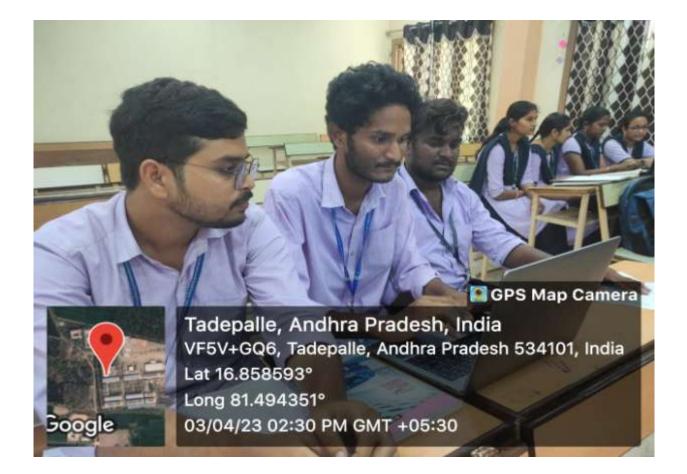


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Tadepalle, Andhra Pradesh, India VF5V+9QH, Tadepalle, Andhra Pradesh 534101, India Lat 16.858566° Long 81.494347° 28/03/23 02:49 PM GMT +05:30

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Department of Electronics & Communication Engineering

PROGRAM EVALUATION FORM

Please fill out this form and return to the Department. This form is only used to evaluate the quality/value of the trainers.

Trainer Name: Mr. U. Uma Maheswara Rao, Research Scholar, NIT, AP

Skill Oriented Program Name: Basic Digital Circuit Design with VHDL and QuestaSim Tool

Date & Time: 27-03-2023 to 01-04-2023

Name of the Organisation: Sri Vasavi Engineering College Branch: ECE

Name of the Student & Reg. No: S. P. V. L. Grayathri & 22185A0417

- (1) The Trainers communicated at an appropriate level for the course. [3]
- (2) The Trainers did a good job of relating course concepts to the real world. [2

(3) The Trainers demonstrated a thorough knowledge of the subject.

- (4) The Trainers were well prepared.
- (5) The Trainers made the class valuable.
- (6) Overall, these Trainers were:

1	2	3	4
Average	Good	Superior	Excellent

	learned ware .	how .	to desig-	n digita	l circuit	s using	Questa-sim
Sugges	tions (if any):					
The	humble	suggesti	on from	n us i	s to pro	vide a	system to
each	student	with	respective	e softwa	re so that	everyon	e can learn t

Signature of the Student

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Mission:

To create a learner centric environment that promotes the intellectual growth of the students.

To develop linkages with R & D organizations and educational institutions for excellence in teaching,

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Skill Oriented Program Name: Basic Digital Circuit Design with VHDL and QuestaSim Tool

Date & Time: 27-03-2023 to 01-04-2023

Name of the Organisation: Sri Vasavi Engineering College Branch: ECE

Name of the Student & Reg. No: Reddy Mohan Srikanth/ 21A81A04I4

- (1) The Trainers communicated at an appropriate level for the course. [3]
- (2) The Trainers did a good job of relating course concepts to the real world. [4]

(3) The Trainers demonstrated a thorough knowledge of the subject.

- (4) The Trainers were well prepared.
- (5) The Trainers made the class valuable.
- (6) Overall, these Trainers were:

1	2	3	4
Average	Good	Superior	Excellent

Key take away points from this one week Program : learned that how to design a logic gates using VHDL learned that testbench codes cleary for different Suggestions (if any): opinion is that the program will continue for 2 more days My to understood clearly. Signature of the Student

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Skill Oriented Program Name: Basic Digital Circuit Design with VHDL and QuestaSim Tool

Date & Time: 27-03-2023 to 01-04-2023

Name of the Organisation: Sri Vasavi Engineering College Branch: ECE

Name of the Student & Reg. No: G1. protap & 21A81A04F0.

- The Trainers communicated at an appropriate level for the course.
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- (2) The Trainers did a good job of relating course concepts to the real world. [4]
- (3) The Trainers demonstrated a thorough knowledge of the subject.
- (4) The Trainers were well prepared.
- (5) The Trainers made the class valuable.
- (6) Overall, these Trainers were:

1	2	3	4
Average	Good	Superior	Excellent

Key take away points from this one week Program: → we learned to able to understand vHDL programme. and implemented programmes like 3x8, decody, full addyet. Suggestions (if any): please -NO. suggestions -

Signature of the Student

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Trainer Name: Mr. U. Uma Maheswara Rao, Research Scholar, NIT, AP

Skill Oriented Program Name: Basic Digital Circuit Design with VHDL and QuestaSim Tool

Date & Time: 27-03-2023 to 01-04-2023

Name of the Organisation: Sri Vasavi Engineering College Branch: ECE

Name of the Student & Reg. No: CH.VAMSI, 21A81A04E0

- (1) The Trainers communicated at an appropriate level for the course.
- (2) The Trainers did a good job of relating course concepts to the real world. [Yes h
- (3) The Trainers demonstrated a thorough knowledge of the subject.
- (4) The Trainers were well prepared.
- (5) The Trainers made the class valuable.
- (6) Overall, these Trainers were:

1	2	3	4
Average	Good	Superior	Excellent

. Learn	to	write	own	vhdl	code	Eits	simula	tion
Rilearn	ed	codes	s on	flip	FIOPS	like D	ETESt	bench cod
Suggestions	(if any):				31			

Signature of the Student

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[Yes]4

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Skill Oriented Program Name: Basic Digital Circuit Design with VHDL and QuestaSim Tool

Date & Time: 27-03-2023 to 01-04-2023

Name of the Organisation: Sri Vasavi Engineering College

Branch: ECE

P. Frencenth Kiemag

Name of the Student & Reg. No: 2148HOUH9

[2] (1) The Trainers communicated at an appropriate level for the course.

(2) The Trainers did a good job of relating course concepts to the real world. [3]

(3) The Trainers demonstrated a thorough knowledge of the subject.

(4) The Trainers were well prepared.

(5) The Trainers made the class valuable.

(6) Overall, these Trainers were:

1	2	3	4
Average	Good	Superior	Excellent

test bench code , architecture Behavioral of counter, Key take away points from this one week Program : IEEE, VHDL, and How to Suggestions (if any): better to give with, better to explain in Signature of the Student

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Trainer Name: Mr. U. Uma Maheswara Rao, Research Scholar, NIT, AP

Skill Oriented Program Name: Basic Digital Circuit Design with VHDL and QuestaSim Tool

Date & Time: 27-03-2023 to 01-04-2023

Name of the Organisation: Sri Vasavi Engineering College Branch: ECE

Name of the Student & Reg. No: 21A 81A04HZ, 5 7. Sabout.

- The Trainers communicated at an appropriate level for the course.
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- (3) The Trainers demonstrated a thorough knowledge of the subject.
- (4) The Trainers were well prepared.
- (5) The Trainers made the class valuable.
- (6) Overall, these Trainers were:

1	2	3	4 🗸
Average	Good	Superior	Excellent

Key take away points from this one week Program: How to design logic gates. Hip Mops and Knowing why we are using some key words in the program. Suggestions (if any):

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Signature of the Student

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Trainer Name: Mr. U. Uma Maheswara Rao, Research Scholar, NIT, AP

Skill Oriented Program Name: Basic Digital Circuit Design with VHDL and QuestaSim Tool

Date & Time: 27-03-2023 to 01-04-2023

Name of the Organisation: Sri Vasavi Engineering College Branch: ECE

B.V.Karthikeya, M.Eswar Bharath. Name of the Student & Reg. No: 21A81A04D9, G5

(1) The Trainers communicated at an appropriate level for the course. [4]

(2) The Trainers did a good job of relating course concepts to the real world. [3

(3) The Trainers demonstrated a thorough knowledge of the subject.

(4) The Trainers were well prepared.

(5) The Trainers made the class valuable.

(6) Overall, these Trainers were:

1	2	3	.4
Average	Good	Superior	Excellent

Key take away points from this one week Program : How to design logic gates, FF's etc., and knowing why we are using keywords in coding. easily understanding how to write Test bench codes. Suggestions (if any):

B.V. Kouthileya

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Signature of the Student

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Skill Oriented Program Name: Basic Digital Circuit Design with VHDL and QuestaSim Tool

Date & Time: 27-03-2023 to 01-04-2023

Name of the Organisation: Sri Vasavi Engineering College Branch: ECE

Name of the Student & Reg. No: 21- 4D4, 4D8, 4E1, 4E3

- The Trainers communicated at an appropriate level for the course.
 [3]
- (2) The Trainers did a good job of relating course concepts to the real world. [4

(3) The Trainers demonstrated a thorough knowledge of the subject.

- (4) The Trainers were well prepared.
- (5) The Trainers made the class valuable.
- (6) Overall, these Trainers were:

1	2	,3/	4
Average	Good	Superior	Excellent

Key take away points from this one week Program : → It is a good course for learning → we felt that, it's a useful course and enjoyed it while learning Suggestions (if any): _) If the programme could be continued box few more days we will learn more

Signature of the Student

[4]

[4

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Skill Oriented Program Name: Basic Digital Circuit Design with VHDL and QuestaSim Tool

Date & Time: 27-03-2023 to 01-04-2023

Name of the Organisation: Sri Vasavi Engineering College Branch: ECE

Name of the Student & Reg. No: M. Meghana 21A81A0467

- (1) The Trainers communicated at an appropriate level for the course. [3
- (2) The Trainers did a good job of relating course concepts to the real world. [3

(3) The Trainers demonstrated a thorough knowledge of the subject.

- (4) The Trainers were well prepared.
- (5) The Trainers made the class valuable.
- (6) Overall, these Trainers were:

1	2	3	4
Average	Good	Superior	Excellent

Key take away points from this one week Program : In this program we know about the VHDL using Questasim tool and we perform oper ations on logic gates Hipflops, Mux, Decoder, register

Suggestions (if any): 'Lto

M-Meghana Signature of the Student

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Skill Oriented Program Name: Basic Digital Circuit Design with VHDL and QuestaSim Tool

Date & Time: 27-03-2023 to 01-04-2023

Name of the Organisation: Sri Vasavi Engineering College Branch: ECE

Name of the Student & Reg. No: M. Sailaja, 21A81A04G3

- (1) The Trainers communicated at an appropriate level for the course. [Yes] 4
- (2) The Trainers did a good job of relating course concepts to the real world. [Yes] 4
- (3) The Trainers demonstrated a thorough knowledge of the subject. [Yes] 3
- (4) The Trainers were well prepared.
- (5) The Trainers made the class valuable.
- (6) Overall, these Trainers were:

Average	Good	Superior	Excellent
1	2	3	4

Key take away points from this one week Program: In this program we learn about VHDL programing and how to white an VHDL cade of rest bench code and also I learn how to use questasion Suggestions (if any): No suggestions.

M. Sailaja. Signature of the Student

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Skill Oriented Program Name: Basic Digital Circuit Design with VHDL and QuestaSim Tool

Date & Time: 27-03-2023 to 01-04-2023

Name of the Organisation: Sri Vasavi Engineering College Branch: ECE

Name of the Student & Reg. No: K.G. T. N. Anjali [21A81A04F7] & N. Kavya 581 [21A81A04G8]

The Trainers communicated at an appropriate level for the course.

(2) The Trainers did a good job of relating course concepts to the real world.

(3) The Trainers demonstrated a thorough knowledge of the subject.

(4) The Trainers were well prepared.

(5) The Trainers made the class valuable.

(6) Overall, these Trainers were:

1	2	3	¥.
Average	Good	Superior	Excellent

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uggestions (if	any):		L ISUT	1000				

k. Anjali"; Nolamp

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Signature of the Student

Vision:

To develop the department into a centre of excellence and produce high quality, technically competent and responsible Electronics and Communication Engineers.

Mission:

To create a learner centric environment that promotes the intellectual growth of the students.

To develop linkages with R & D organizations and educational institutions for excellence in teaching, learning and consultancy practices.

SRI VASAVI ENGINEERING COLLEGE (AUTONOMOUS)

(Sponsored by Sri Vasavi Educational Society) (Approved by AICTE, New Delhi & Recognized by UGC under section 2(f) & 12(B)) (Permanently affiliated to JNTUK, Kakinada, Accredited by NBA and NAAC with 'A' Grade) Pedatadepalli, TADEPALLIGUDEM - 534 101.W.G.Dist. (A.P)

Department of Electronics & Communication Engineering

PROGRAM EVALUATION FORM

Please fill out this form and return to the Department. This form is only used to evaluate the quality/value of the trainers.

Trainer Name: Mr. U. Uma Maheswara Rao, Research Scholar, NIT, AP

Skill Oriented Program Name: Basic Digital Circuit Design with VHDL and QuestaSim Tool

Date & Time: 27-03-2023 to 01-04-2023

Name of the Organisation: Sri Vasavi Engineering College Branch: ECE

sirisha Name of the Student & Reg. No: p. likhitha [21A81A04H9], SN: P. Vijaya lakshmi [4I6], S. 418

- (1) The Trainers communicated at an appropriate level for the course.
- (2) The Trainers did a good job of relating course concepts to the real world. [/]
- (3) The Trainers demonstrated a thorough knowledge of the subject.
- (4) The Trainers were well prepared.
- (5) The Trainers made the class valuable.
- (6) Overall, these Trainers were:

1	2	3	4
Average	Good	Superior	Excellent

Key take away points from this one week Program : we have learned few more things about VH DL we got some idea about questasimsoftware. Suggestions (if any):

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Signature of the Student

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Department of Electronics & Communication Engineering

PROGRAM EVALUATION FORM

Please fill out this form and return to the Department. This form is only used to evaluate the quality/value of the trainers.

Trainer Name: Mr. U. Uma Maheswara Rao, Research Scholar, NIT, AP

Skill Oriented Program Name: Basic Digital Circuit Design with VHDL and QuestaSim Tool

27-03-2023 to 01-04-2023 Date & Time:

Name of the Organisation: Sri Vasavi Engineering College Branch: ECE

Name of the Student & Reg. No: G.L. Sowjanya [21ASIA04E8] & S.Vijaya [21A 81A04J3

- (1) The Trainers communicated at an appropriate level for the course.
- (2) The Trainers did a good job of relating course concepts to the real world. [
- (3) The Trainers demonstrated a thorough knowledge of the subject.
- (4) The Trainers were well prepared.
- (5) The Trainers made the class valuable.
- (6) Overall, these Trainers were:

1	2	3	(4)
Average	Good	Superior	Excellent

Key take away points from this one week Program : we learnt how to write VHDL code & how to stimulate it.

Suggestions (if any):

Soujanya,

Signature of the Student

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Date & Time: 27-03-2023 to 01-04-2023

Name of the Organisation: Sri Vasavi Engineering College Branch: ECE

Name of the Student & Reg. No: P. Asritha, R1A81A04H5

- (1) The Trainers communicated at an appropriate level for the course. [4
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- (6) Overall, these Trainers were:

1	2	3	4
Average	Good	Superior	Excellent

Key take away points from this one week Program: Got a brief understanding on implementing and to write a VHDL code.

Suggestions (if any):

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Name of the Organisation: Sri Vasavi Engineering College Branch: ECE

Name of the Student & Reg. No: p. 11khitha [21A81A04H9], SN: P.VIJaya lakshmi [416], S. Sirisha

- (1) The Trainers communicated at an appropriate level for the course.
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Certification of Participation

U. Una Mahren Rea Research scholar, NIT, AP

E. Kumaling. HOD. ECE



Certification of Participation

This certificate is presented to .Satti Nacya Pacima Vijaya Lakshmi. studyingyear B. Tech in <u>ECE</u> branch for active participation one week Skill Oriented Program on "Basic Digital Circuit Design with VHDL and QuestaSim Tool" conducted by Department of Electronics & Communication Engineering from 27-03-2023 to 01-04-2023 under Scheme for Promotion of Interests, Creativity & Ethics among Students (SPICES), sponsored by AICTE

1). Una Mahren fre Trainer. Research scholar, NIT, AP

E. Kusmaline. HOD, ECE

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Certification of Participation

This certificate is presented to Sanku. Chitu. V.N.S.S. Vata. Prasacl...... studyingyear B. Tech inbranch for active participation one week Skill Oriented Program on "Basic Digital Circuit Design with VHDL and QuestaSim Tool" conducted by Department of Electronics & Communication Engineering from 27-03-2023 to 01-04-2023 under Scheme for Promotion of Interests, Creativity & Ethics among Students (SPICES), sponsored by AICTE

1). Una Maherin fear

Trainer, Research scholar, NIT, AP

E. Kumalue. HOD. ECE



Certification of Participation

U. Una Mahren Rea Trainer. Research scholar, NIT, AP

E. Kumalina. HOD. ECE



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Trainer, Research scholar, NIT, AP

E. Kumalin HOD. ECE



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Certification of Participation

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E. Kumaline. HOD, ECE

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E. Kumaline. HOD. ECE

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1). Una Mahren Pear Trainer, Research scholar, NIT, AP

E. Kumaline. HOD, ECE



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Trainer, Research scholar, NIT, AP

E. Kumaline HOD. ECE

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This certificate is presented to<u>Marri Eswar Bharath</u> studying!!.....year B. Tech in<u>ECE</u>....branch for active participation one week Skill Oriented Program on "Basic Digital Circuit Design with VHDL and QuestaSim Tool" conducted by Department of Electronics & Communication Engineering from 27-03-2023 to 01-04-2023 under Scheme for Promotion of Interests, Creativity & Ethics among Students (SPICES), sponsored by AICTE

1). Una Mahen Hear Trainer. Research scholar, NIT, AP

E. Kumaline. HOD, ECE